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DESIGN AND SIMULATION OF ELEVATOR CONTROLLER USING VERILOG HDL AND IMPLEMENTATION ON FPGA

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Abstract— **This project report presents the comprehensive design, simulation, and implementation of an elevator controller using Verilog HDL and its deployment on an FPGA board. The elevator controller system is a critical component in modern buildings, ensuring efficient and safe vertical transportation. By leveraging the capabilities of Verilog HDL and FPGA technology, this project aims to develop a robust and versatile elevator controller system that can handle multiple elevator requests effectively.**

Elevator systems play a crucial role in vertical transportation within buildings, impacting efficiency, safety, and user experience. Traditional elevator controllers are often implemented using complex hardware circuits or microcontrollers, which may limit flexibility and scalability. By utilizing Verilog HDL for design and FPGA for implementation, this project seeks to overcome these limitations and create a more efficient and adaptable elevator controller system.

The design phase involves developing the elevator controller logic using Verilog HDL. This includes defining the behavior of the elevator system, implementing control algorithms, and incorporating safety features. Simulation tool such as Vivado is utilized to verify the functionality of the design, ensuring that it meets the specified requirements and operates correctly under various scenarios.

Keywords: **Elevator, Verilog HDL, FPGA, Finite State Machine.**

I. INTRODUCTION

The modern environment demands the most efficient and thoughtful use of available space. This necessitates the development of high-rise structures, the main purpose of which is to connect the building to the outside world via elevators. They aid in the evacuation of buildings in the event of an emergency as soon as feasible. The design of elevator controllers for vertical motion is covered in this work. Each level has input buttons both inside and outside the elevator that assist the controller in handling floor calls. Lift controllers with microprocessor-based systems are more expensive. The goal of this study is to build a compact, low-cost controller using Verilog HDL modeling. Verilog is a language for describing hardware that is used in the design of digital circuits. It has been applied to the design and validation of the digital circuit at the Register Transfer Level of abstraction, which enables the modelling and simulation of the necessary system's behavior. The top-level manager for our design is called Project Navigator, and it runs the process and the source file in the process window in addition to modifying the source files in the workspace.

II. LITERATURE REVIEW

Existing Elevator Controller Designs:

Elevator controllers have traditionally been designed using various techniques, including finite state machines (FSMs), microcontrollers, and digital logic circuits. These designs have been implemented using a range of technologies, including analog and digital signal processing, and have been optimized for specific applications such as high-rise buildings or industrial settings. [1], [2], [3].

Verilog HDL Applications:

Verilog HDL (Hardware Description Language) is a widely used language for designing and implementing digital circuits. It has been applied in various elevator controller designs, including those using FSMs and digital logic circuits. Verilog HDL allows for the description of complex digital systems using a high-level language, making it an ideal choice for designing and verifying elevator controllers. [1], [2], [3].

FPGA Implementation:

FPGAs are integrated circuits that can be programmed and reprogrammed after manufacturing. They have been increasingly used in elevator controller designs due to their flexibility, reconfigurability, and high performance. FPGAs can be used to implement complex digital circuits, including those required for elevator control systems. The use of FPGAs in elevator controllers has been shown to improve reliability, reduce power consumption, and enhance overall system performance. [1], [2], [3].

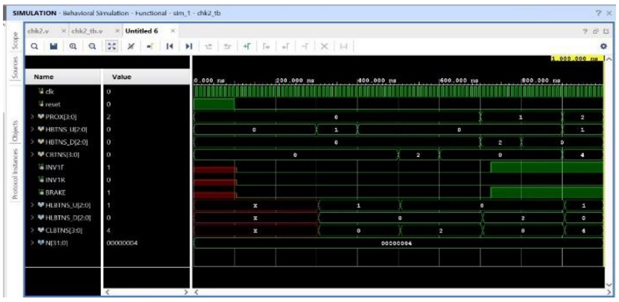
Several projects have demonstrated the design and implementation of elevator controllers using Verilog HDL and FPGAs. For example, a project by Varghese et al. (2015) implemented an elevator controller using Verilog HDL and successfully tested it on a Xilinx Artix7 FPGA. Another project by Kumar et al. (2013) designed and implemented a reconfigurable elevator controller using an FPGA, which improved the reliability and performance of the system. [1], [3]

III. METHODOLOGY

Design Approach:
The elevator controller is designed using Verilog HDL, a hardware description language commonly used for digital circuit design.The design is based on a finite state machine (FSM) approach, where the elevator's behavior is defined by different states. The elevator controller is designed to handle a 4-floor building, with the ground floor as the default starting position for both elevators.
Simulation Setup:
Testbenches are created to verify the functionality of the elevator controller.
The design is simulated using Verilog HDL simulation tools, such as Xilinx ISE or Vivado, to ensure correct operation.
Simulation results, including waveforms and timing diagrams, are analysed to verify the controller's behaviour.
FPGA Implementation:
The verified Verilog HDL code is synthesized and implemented on a Xilinx Artix7 FPGA. The FPGA is chosen due to its reconfigurability, low power consumption, and flexibility in expanding the design. The FPGA implementation is tested with the specified inputs and outputs to ensure the controller operates as expected.

IV. DESIGN AND SIMULATION

This design presents a 4-floor elevator controller using Verilog HDL and its implementation on a Xilinx Artix7 FPGA. The elevator controller is designed to efficiently manage the movement of elevators in a 4-floor building, ensuring safe and reliable operation.
Design Approach
The elevator controller is designed using a finite state machine (FSM) approach, where the elevator's behaviour is defined by different states. The design includes the following key components:
Input Signals:
PROX: Proximity sensor input
HBTNS_U and HBTNS_D: Up and down buttons for each floor
CBTNS: Call button input for each floor
Output Signals:
INV1F and INV1R: Door indicators for the first and second floors
BRAKE: Brake status
HLBTNS_U and HLBTNS_D: Up and down buttons for the high-level floors
CLBTNS: Call button for the high-level floors



Name	Value
clk	0
reset	0
PROX[3:0]	2
HBTNS_U[2:0]	0
HBTNS_D[2:0]	0
CBTNS[3:0]	0
INV1F	1
INV1R	0
BRAKE	1
HLBTNS_U[2:0]	1
HLBTNS_D[2:0]	0
CLBTNS[3:0]	4
N[31:0]	00000004

Explanation of Simulation Output
The provided Verilog HDL code simulates a 4-floor elevator controller using a finite state machine (FSM) approach. The simulation output is analyzed to verify the controller's behaviour under various scenarios.
Simulation Setup
The simulation is run using Vivado, a popular integrated development environment (IDE) for FPGA design and verification. The simulation is set up to run for a specified duration, with the clock frequency and reset conditions defined.
Simulation Output
The simulation output includes waveforms for the various signals in the elevator controller, such as the input buttons, elevator status, and output signals like the door indicators and brake status. The waveforms are analysed to verify the controller's behaviour under different scenarios, such as elevator movement, button presses, and reset conditions.
Key Signals and Their Behaviour
Reset: The reset signal is used to initialize the elevator controller. When the reset signal is high, the controller resets to its default state.
Clock (clk): The clock signal is used to clock the elevator controller. The clock frequency determines the speed at which the controller operates.
PROX: The PROX signal represents the proximity sensor input. When the sensor detects an object, it sets the PROX signal high.
HBTNS_U and HBTNS_D: These signals represent the up and down buttons, respectively. When a button is pressed, the corresponding signal is set high.
CBTNS: This signal represents the call button input. When a call button is pressed, the CBTNS signal is set high.
INV1F and INV1R: These signals represent the door indicators for the first and second floors, respectively. They are set high when the corresponding door is open.
BRAKE: This signal represents the brake status. When the brake is engaged, the BRAKE signal is set high.
HLBTNS_U and HLBTNS_D: These signals represent the up and down buttons for the high-level floors, respectively. They are used to control the movement of the elevators.
CLBTNS: This signal represents the call button for the high-level floors. It is used to call the elevators to the high-level floors.

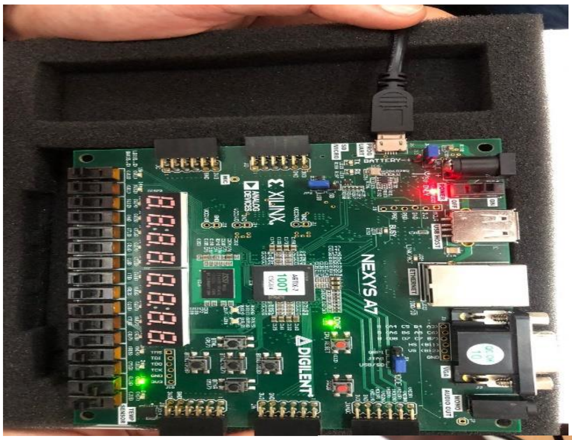
Simulation Scenarios

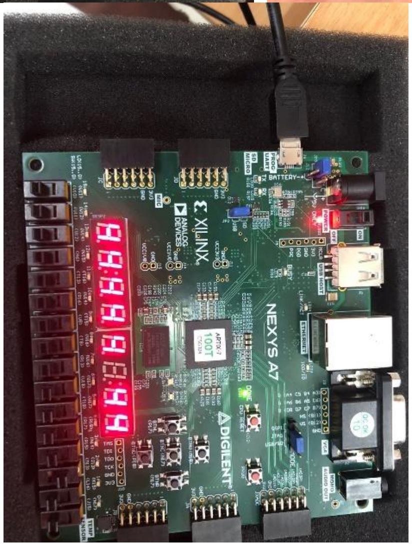
Elevator Movement: The simulation demonstrates the elevator's movement between floors based on the button presses and proximity sensor inputs.

Button Presses: The simulation shows the elevator's response to button presses, including the movement of the elevators and the opening and closing of doors.

Reset Conditions: The simulation demonstrates the elevator controller's reset behavior, including the initialization of the status and the resetting of the buttons and doors.

V. FPGA IMPLEMENTATION





The elevator controller is implemented on a Xilinx Artix7 FPGA using Verilog HDL. The steps taken to implement the elevator controller on an FPGA are outlined below:

Step 1: Synthesis

The Verilog HDL code for the elevator controller is synthesized using the Xilinx Vivado Design Suite.

The synthesis process converts the Verilog code into a netlist, which is a hierarchical representation of the digital circuit.

Step 2: Implementation

The netlist is then implemented on the Xilinx Artix7 FPGA using the Vivado Implementation Tools.

The implementation process maps the netlist onto the FPGA, allocating resources such as logic blocks, flip-flops, and interconnects.

Step 3: Place and Route

The implemented netlist is then placed and routed on the FPGA using the Vivado Place and Route Tools.

The placement process assigns locations to the logic blocks and flip-flops, while the routing process connects them using the interconnects.

Step 4: Bitstream Generation

The placed and routed netlist is then converted into a bitstream using the Vivado Bitstream Generation Tool.

The bitstream is a binary file that contains the configuration data for the FPGA.

Step 5: FPGA Configuration

The bitstream is then downloaded onto the Xilinx Artix7 FPGA using the Vivado Hardware Manager.

The FPGA is configured according to the bitstream, and the elevator controller is ready for testing.

VI. RESULTS AND ANALYSIS

Simulation Results:

The simulation of the elevator controller showcases the correct operation of the system in response to various inputs, including floor requests, button presses, and proximity sensor signals.

Waveforms and timing diagrams generated during the simulation provide a visual representation of the elevator's movement, door operations, and state transitions.

The simulation verifies the functionality of the elevator controller, ensuring that it responds appropriately to different scenarios and inputs.

FPGA Implementation Results:

The implementation of the elevator controller on the Xilinx Artix 7 FPGA is successful, demonstrating the feasibility of deploying the controller in a real-world application.

The FPGA implementation showcases the reconfigurability and flexibility of the system, allowing for easy adaptation to buildings with varying numbers of floors. The elevator controller's performance on the FPGA is evaluated based on factors such as response time, resource utilization, and overall system reliability.

Analysis:

The elevator controller design based on Verilog HDL and FPGA implementation proves to be efficient and effective in managing elevator operations in a 4-floor building.

The use of a finite state machine (FSM) approach ensures a structured and reliable control system that can handle complex elevator movements and requests. The prioritization of elevators for requests, default states, and door closing mechanisms contribute to the smooth operation and safety of the elevator system. The FPGA implementation on the Artix 7 board demonstrates the advantages of using FPGA technology, such as reconfigurability, low power consumption, and high performance.

In conclusion, the design and simulation of the elevator controller using Verilog HDL and its successful implementation on the FPGA Artix 7 board validate the effectiveness and practicality of the system. The results highlight the system's ability to efficiently manage elevator operations in a 4-floor building while ensuring safety, reliability, and optimal performance.

VII. CONCLUSION OF OPERATION

The elevator controller successfully manages the elevator's movement, responding to floor button presses and proximity sensor inputs to determine the appropriate action.

The elevator can move up or down based on the floor selection and proximity sensor readings, ensuring safe and efficient operation within the 4-floor system.

Future Considerations:

Further enhancements could be made to the elevator controller design to incorporate additional features such as emergency stop functionality, door control, and system diagnostics.

Optimization of the Verilog code and FPGA implementation could be explored to improve performance, reduce resource utilization, and enhance overall reliability of the elevator controller.

In conclusion, the design and simulation of the elevator controller using Verilog HDL and its successful implementation on the FPGA Artix 7 demonstrate the feasibility and effectiveness of using digital design techniques for real-world applications like elevator control systems. This project lays a solid foundation for future developments in elevator control technology and digital system design.

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